High Power Microwave Static Induction Transistor

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ABSTRACT

A new type of the transistor called " Static Induction Transistor (SIT)", based on a short channel vertical J-FET structure, has been successfully verified as a promising device for microwave high power operation. The experimental transistors we fabricated have demonstrated the following remarkable features; (1) f_{max} of above 5 GHz, (2) amplifying output power of 13 watts at 1 GHz and (3) oscillating output power of 100 watts at 200 MHz. These data are the highest among any reported FET transistors at this frequency range.

INTRODUCTION

The needs for high power solid state devices operating at microwave frequencies have been increasing in the communication field. At present, bipolar transistors operating at 1 GHz with a power of 40 watts have been reported. However, the power performance at this frequency is near the tchnical limit.

A new type of transistor called " Static Induction Transistor (SIT) " was proposed by J. Nishizawa [1),2)] as a device expected to break through the above limit. The structure is similar to a vertical J-FET, except very short channels, as shown in Fig. 1(a). In a conventional J-FET, the channel resistance is controlled by gate voltage. In SIT, majority carriers are injected into the depleted regions surrounded by gate regions and controlled by electric fields of drain voltage as well as of gate voltage. SIT is expected to exceed bipolar transistors with respect to frequency and power by the following reasons:

(1) Because of small charging and discharging time constants resulted from the short channel structure, SIT is suitable for high frequency operation

(2) Because of higher drift velocity of majority carriers accelerated by high electric field in SIT than the diffusion velocity of minority carriers in bipolar transistors, it is possible to use a longer source-drain distance than the base width in bipolar transistor for any particular frequency. Longer source-drain distance makes breakdown voltage higher. SIT can, therefor, be operated at higher voltage than bipolar transistors.

(3) Negative temperature coefficient of drain current at high current level makes SIT thermally stable at high power operation.

In spite of such great expectation, the output power reported so far is relatively low.[3),4)] Here, we demonstrate the output power of 100 watts range by optimizing the design parameters and adopting a novel structure and process technique.

DESIGN AND FABRICATION OF SIT

To obtain high frequency devices, shorter transit time of carriers and higher figure of merit $Gm/2\pi C$ are desirale. Here, Gm is a mutual conductance and C includes capacitances C_{g-d} between gate and drain and C_{g-s} between gate and source.

Transit time should be as short as 10^{-10}sec, when SIT operates at 1 GHz. It is given by the ratio of source-drain distance and carrier drift velocity. In our experiments, drain current showed $T^{-1/2}$ temperature dependence in the relatively high current level. This temperature dependence coincides with the temperature dependence of the saturation velocity. The carrier drift velocity was , therefore, found to be the saturation velocity. It is known to be 10^{7} cm/sec. The source-drain distance has to be shorter than 10^{-3}cm..

In our experiments, Gm was found to be proportional to donor concentration N_d in the channel region and C was proportional to $N_d^{1/2}$.

The figure of merit, therefore, increases with $N_d^{1/2}$.

For high power operation, it is advantageous to operate at higher voltage and higher current. The breakdown voltage BV_{g-d} between gate and drain decreases with N_d, while it increases with source-drain distance L. This tendency is opposit to that of the frequency characteristics of SIT.

For short transit time 10^{-10}sec, high operating voltage (> 100 volts) and high figure of merit, N_d and L were optimized to 5×10^{14} cm^{-3} and 10^{-3} cm, respectively. Another way to raise BV_{g-d} and to decrease C_{g-d} was to adopt a novel structure in the impurity profile. The donor concentration of drain region was made smaller than that of channel region, as shown in Fig. 1(a).

In addition, to raise the breakdown voltage BV_{g-s} and to decrease the capacitance C_{g-s} between gate and source, step structure between gate and source was fabricated by selective oxidation process.

An SIT was consisted of 8 cells, each of which was consisted of 30 fingers of gate and source interconnections, as shown in Fig. 1(b). The gate width (or source length) was designed to be 2.25 cm so that the drain dissipation power was 20 to 30 watts.

Typical electrical properties of the SIT were shown in Table 1. BV_{g-d} was 130-150 volts, C_{g-d} was 8-9 pFs, C_{g-s} was 20-22 pFs. I-V characteristic of the SIT was triode-like, as shown in Fig. 2. Voltage amplification factor μ was 15-16 and mutual conductance Gm was 70-80 m℧.

HIGH POWER OPERATION AT HIGH FREQUENCY

From the observed scattering parameters, unilateral power gain U, the maximum stable power gain MSG and the maximum available power gain MAG were estimated and shown in Fig. 3. The maximum available oscillating frequency f_{max} was estimated to be above 5 GHz and the MAG at 1 GHz was 5 dB.

The power amplification characteristic at 1 GHz was evaluated by one stage amplifier and shown in Fig. 4. The applied drain voltage was 120 volts and gate voltage was -6.85 volts. The output power was linear up to 10 watts with gain of 3 dB and the maximum output power was 13 watts. This power level is believed to be the maximum value operated at 1 GHz by SIT at present.

SIT has self thermal balancing effect originated from the negative temperature coefficient of drain current. The temperature distribution on the surface of an SIT chip was relatively uniforme and was symmetrical to center line as shown in Fig.5. The temperature distribution was measured under the codition of input DC power of 10 watts and oscillating output power of 0.55 watts at 195 MHz. The maximum temperature difference in active area was about 15 °C.

It has been shown that the power combination by parallel chips operation in one package was easily performed. For example, a combined power at 100 MHz oscillation of 4 chips in one package was 77 watts with 40 % efficiency. Here, the output power of one chip was 20 watts with 44 % efficiency at 100 MHz oscillation. Oscillating output power of 100 watts at 200 MHz was also obtained by a push-pull oscillator with a pair of 3 chips, as shown in Fig.6. Applied drain voltage was 120 volts and drain current was 2.5 amperes at the maximum output condition. The power efficiency was 36 % at output power of 100 watts. In these oscillator, the gate voltage swings to a positive level and the drain current is high as the broken line showed in Fig.2.

Higher power at 1 GHz is expected by an improved design of package and a wiring technique of chips in a package.

CONCLUSION

A high power SIT, 13 watts at 1 GHz with a good linearity, was realized. Successful parallel operations of the SITs, i.e., 77 watts at 100 MHz with 4 chips and 100 watts at 200 MHz with 6 chips, were performed. From these results, it is expected to perform more than 100 watts at frequencies in UHF range near future.

ACKNOWLEDGMENTS

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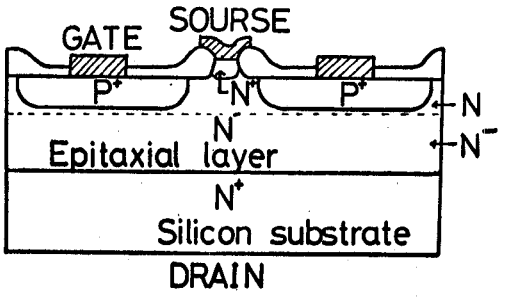
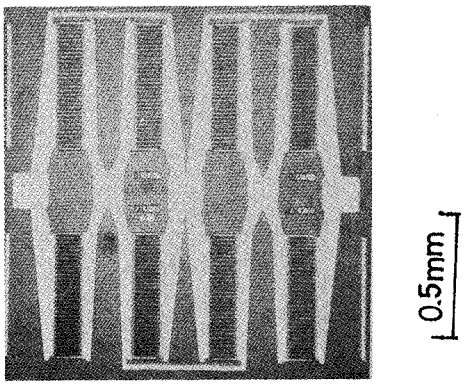
BV_{g-s}	23 - 28 V
BV_{g-d}	130 - 150 V
C_{g-s} (at 10 V)	20 -22 pF
C_{g-d} (at 60 V)	8 - 9 pF
Gm	70 - 80 m℧
μ	15 - 16

Table 1. Electrical properties of SIT



(a) Sectional view of an SIT



(b) Top view of an SIT chip

Fig.1 Schematic diagram of an SIT

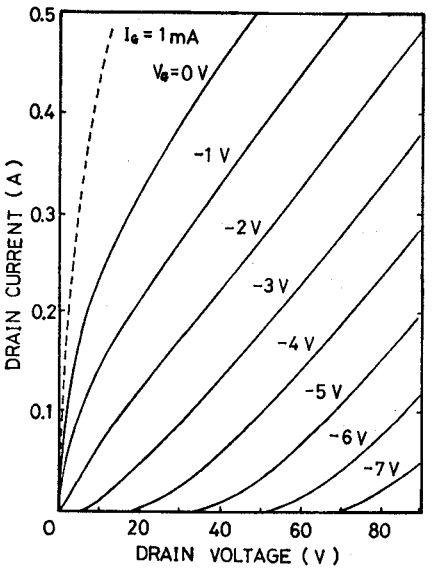


Fig. 2 I-V characteristics of an SIT

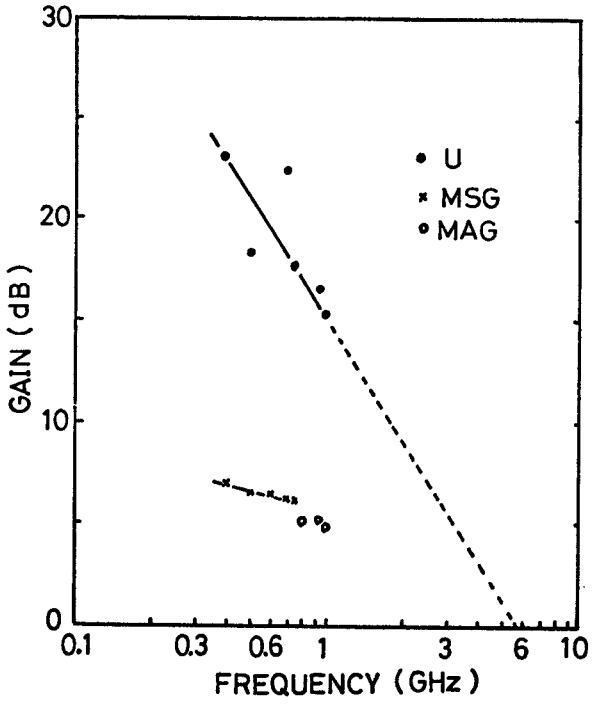
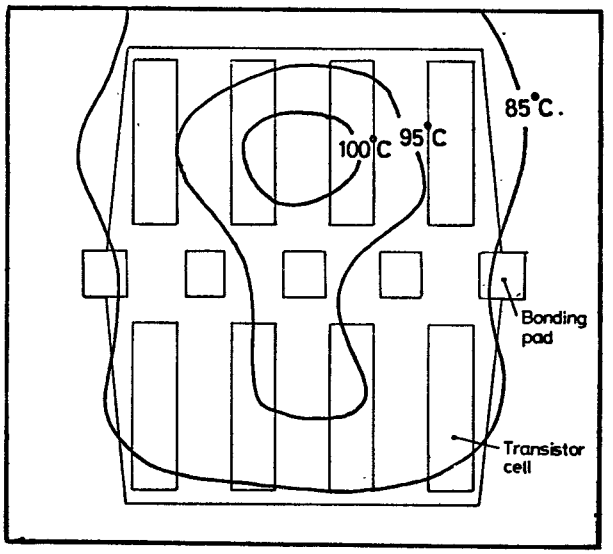


Fig.3 Frequency dependence of U, MSG, and MAG of an SIT



DC input power 10 W
RF output power 0.55 W
(195 MHz oscillation)

Fig.5 Temperature distribution on an SIT chip

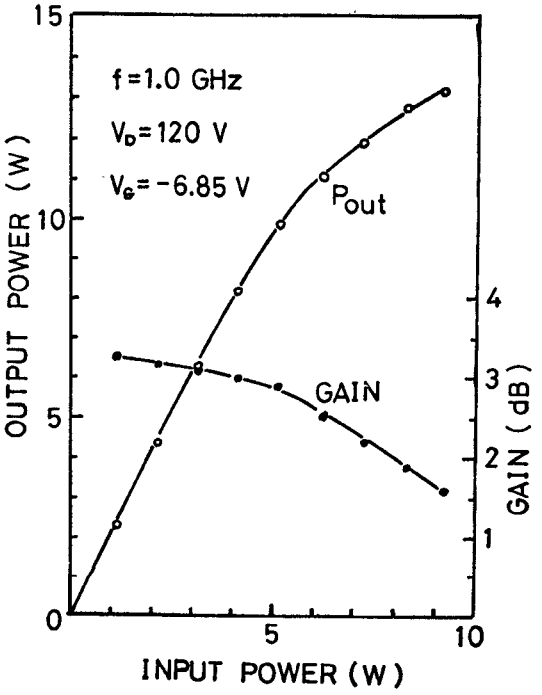


Fig. 4 Amplifier characteristics at 1 GHz

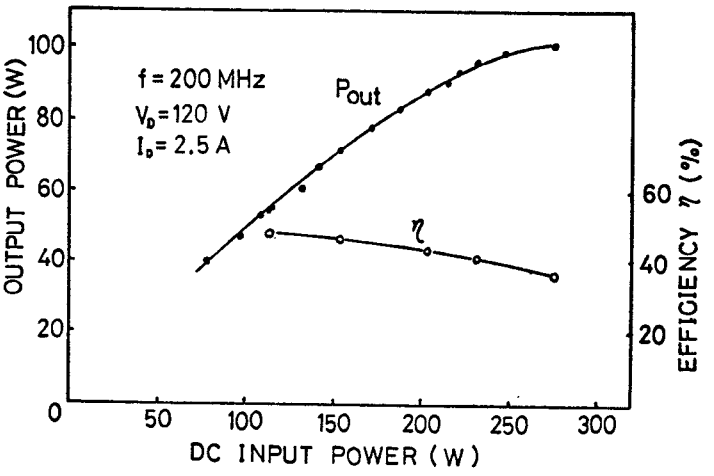


Fig.6 Output power of a push-pull SIT oscillator